A CMOS-Compatible Fabrication Process for Scaled Self-Aligned InGaAs MOSFETs

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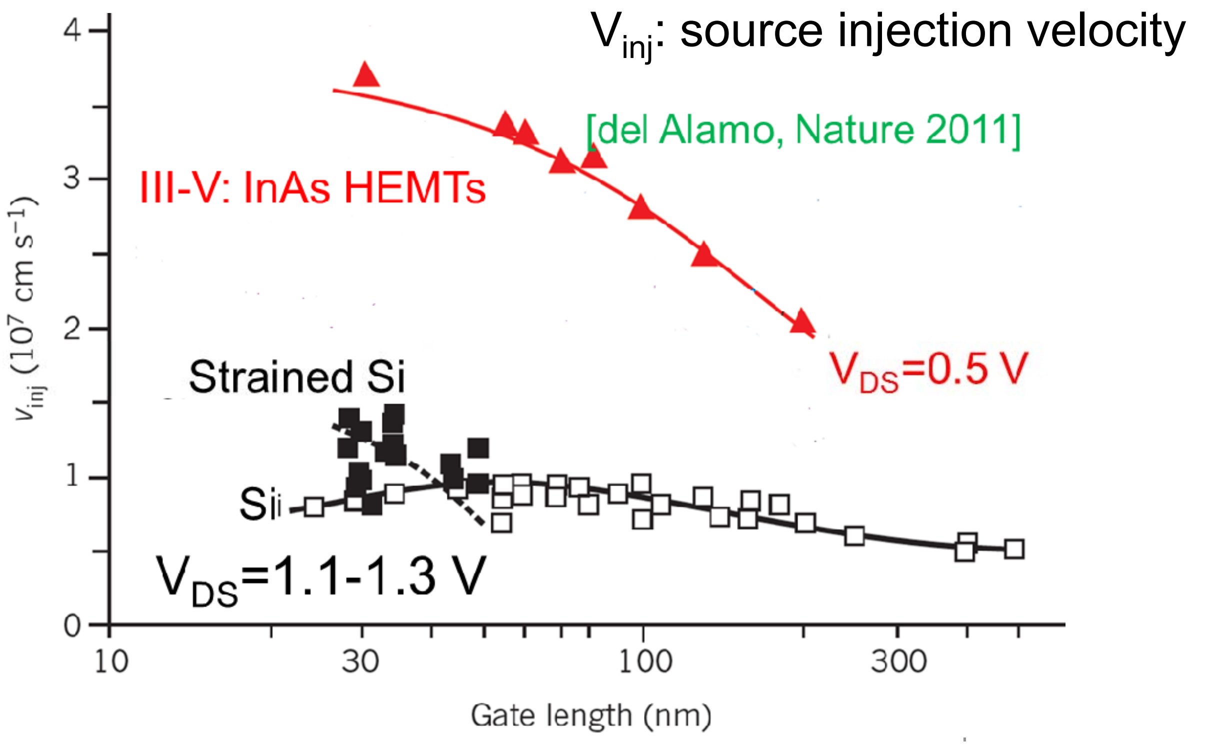
DTRA
NSF E3S STC
MIT SMART program

Motivation for III-V CMOS

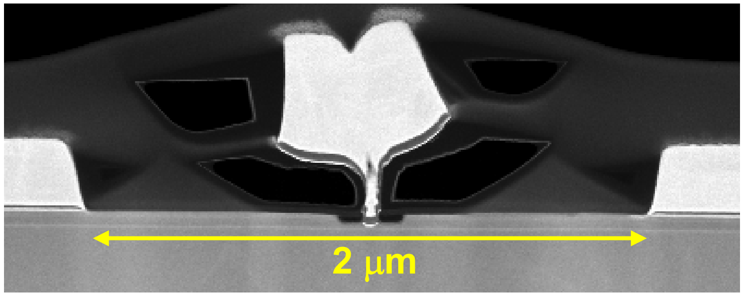
- Superior electron transport properties for III-Vs



- III-V's: promising to extend Moore's Law
- Focus of this talk: InGaAs MOSFET fabrication technology

Self-aligned recessed-gate QW-MOSFET

HEMTs

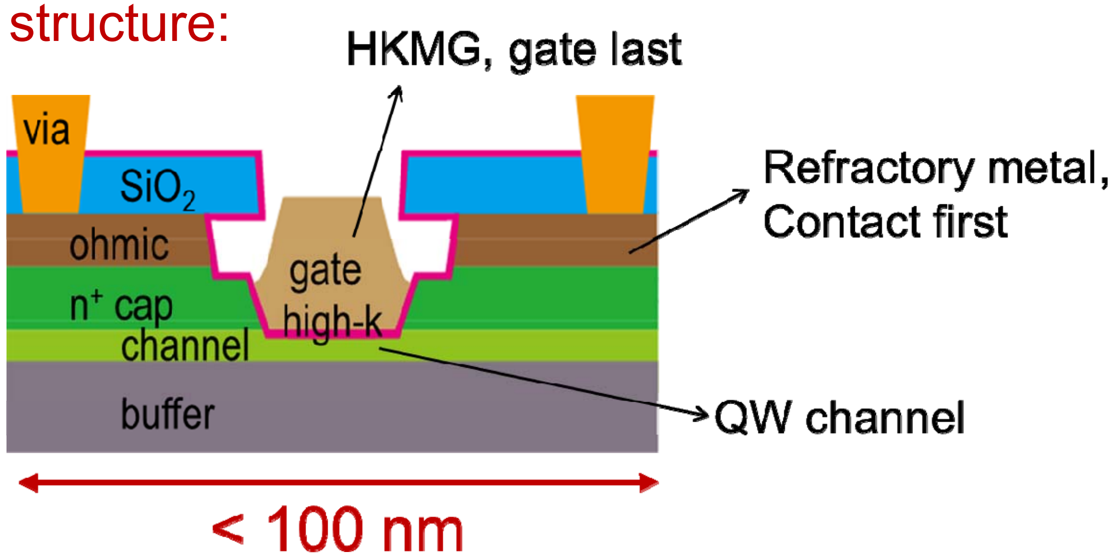


[Kim IEDM 2011]

Considerations for III-V MOSFETs

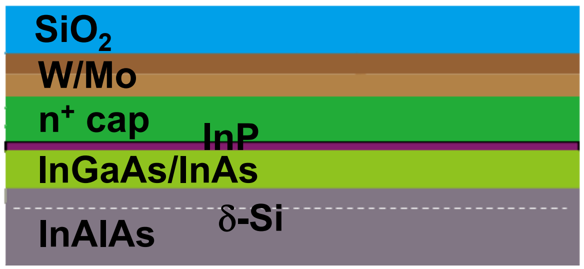
- Gate insulator
  - thin with low leakage, low D_{it}
- High-level self-alignment
  - ohmic metal, access region, gate
- CMOS compatibility
  - free of wet-etch, lift-off and Au

Proposed MOSFET structure:

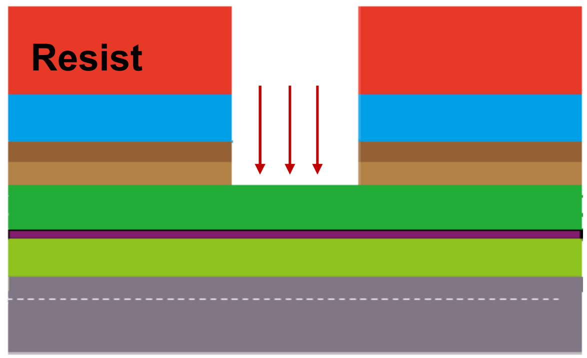


Process overview

Mo/W ohmic contact

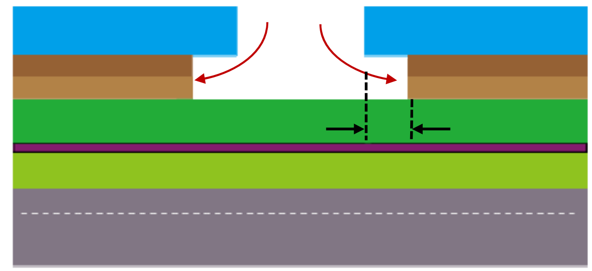


CF_4, SF_6 anisotropic RIE



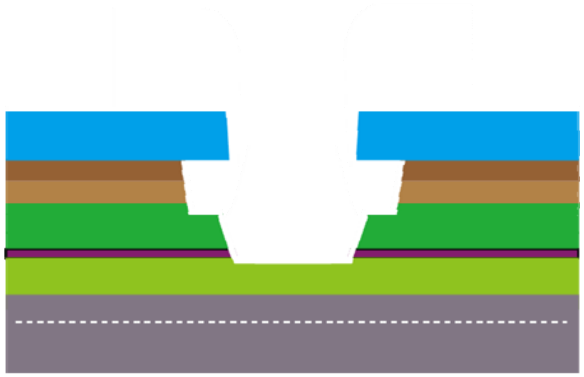
[Lin, APEX 2012]

CF_4+O_2 isotropic RIE

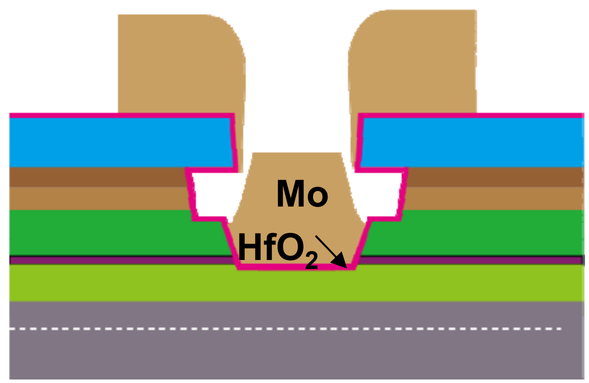


[Lin, IEDM 2013]
[Waldron, IEDM 2007]

III-V recess

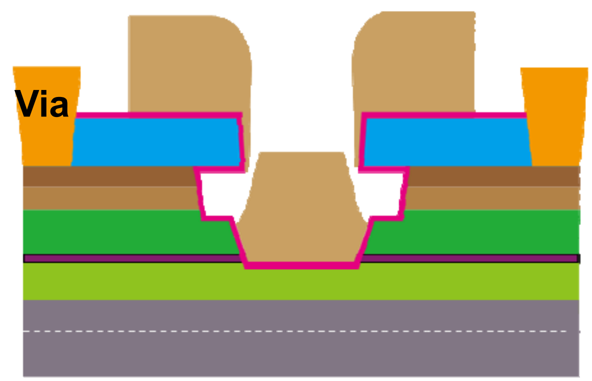


Gate stack

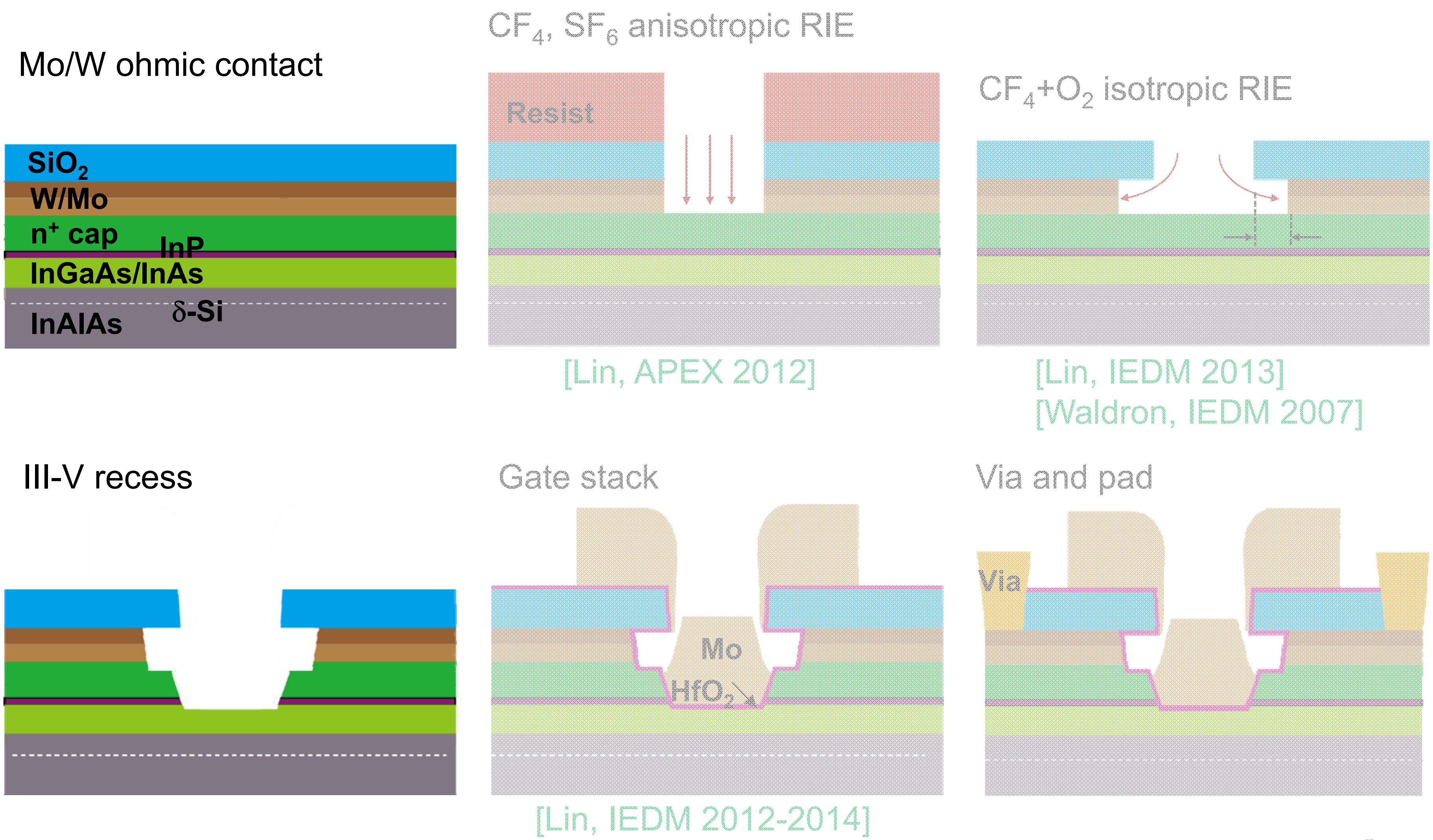


[Lin, IEDM 2012-2014]

Via and pad

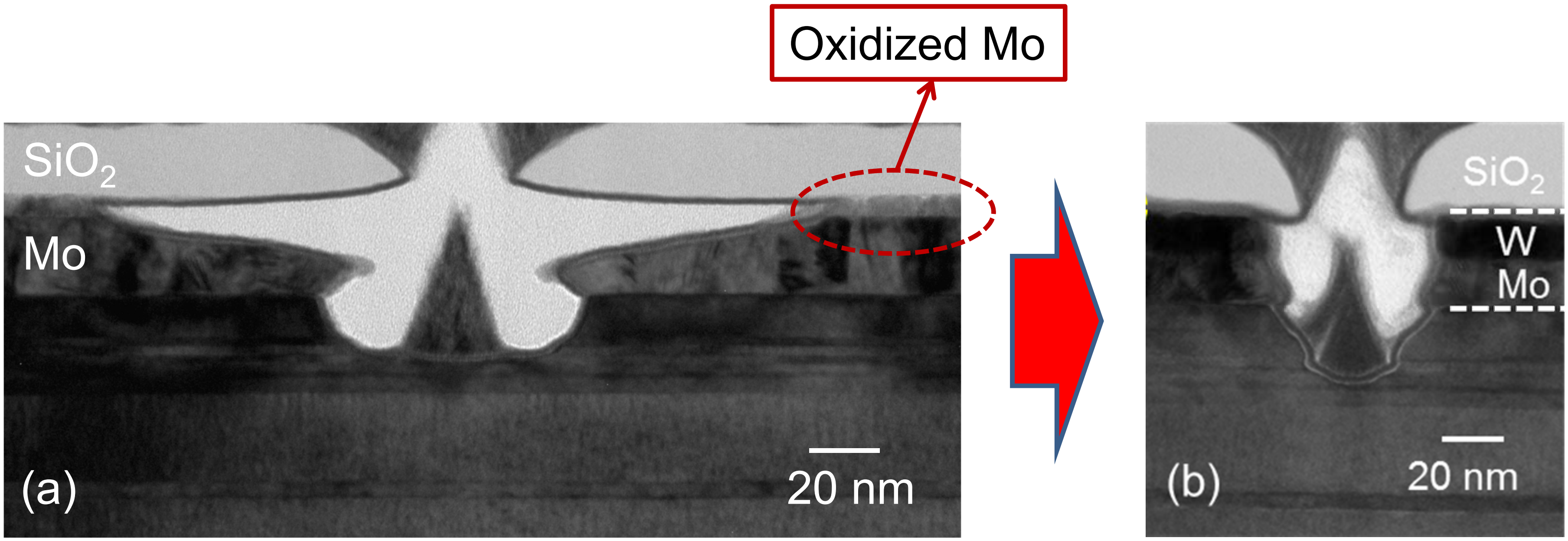


Details of contact and III-V recess processes



W barrier for undercut immunity

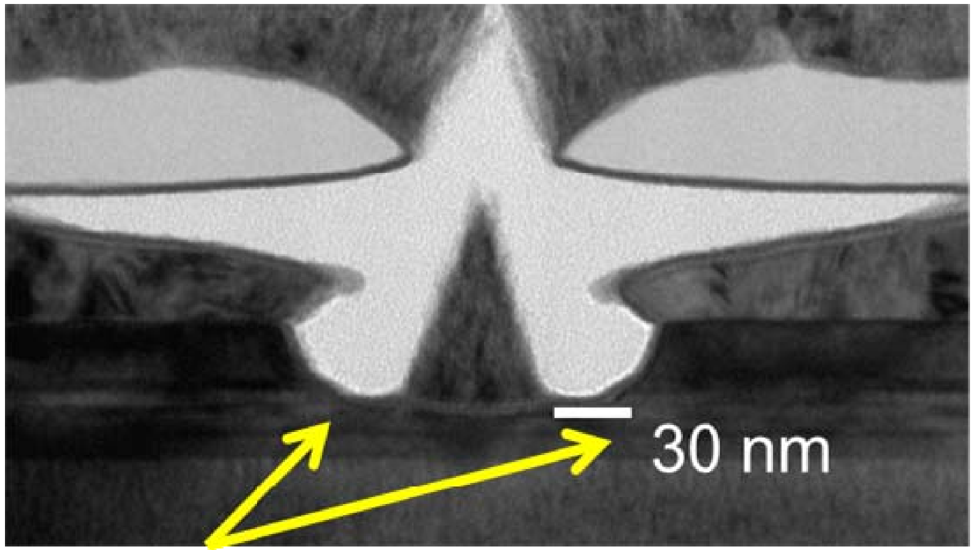
Goal: to reduce device footprint and gate pitch size



[Lin, IEDM 2012]

[Lin, IEDM 2013]

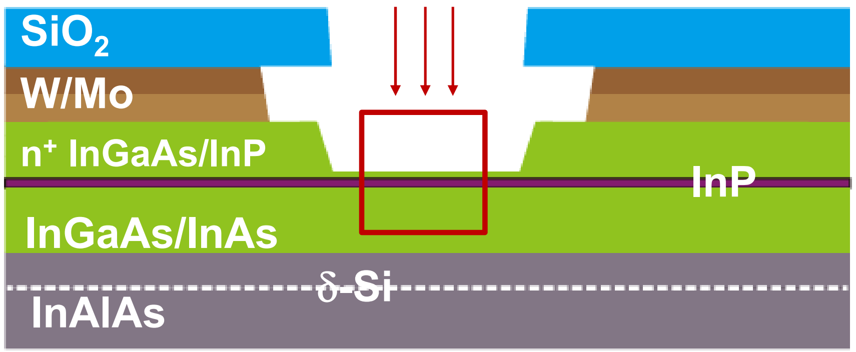
Problems with wet etch gate recess



- Isotropic wet etch → large lateral extent
  - Large footprint
  - Ungated and uncapped access regions → access resistance ↑

New III-V recess technology: Precise channel thickness (t_c) control

Cl_2 anisotropic RIE



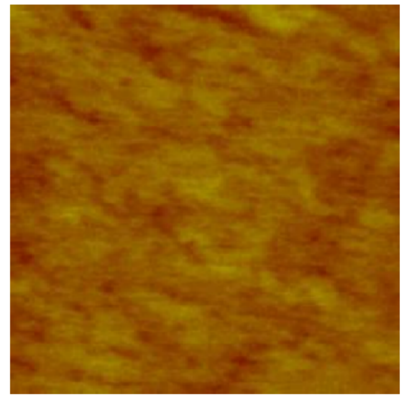
- Anisotropic

III-V dry etch: surface roughness
Selected chemistry Cl_2:N_2

Key parameters:

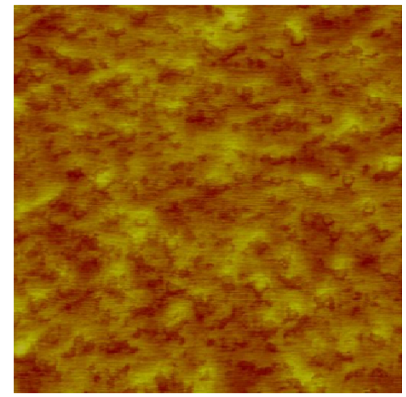
- Bias
- Pressure
- Gas ratio (Cl_2:N_2)
- Gas chemistry

As-grown



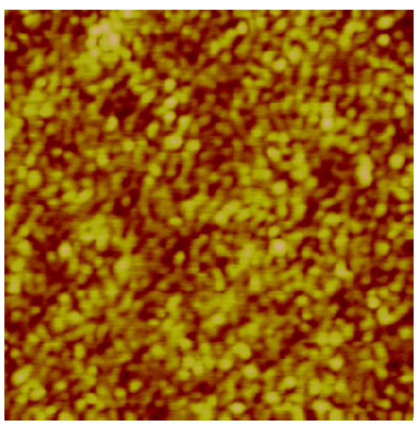
Virgin
RMS: 0.17 nm

Selected recipe

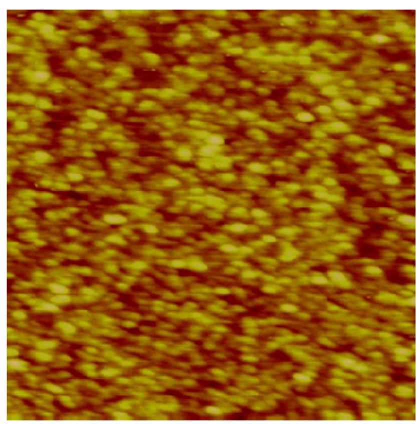


Cl_2:N_2=10:3
RMS: 0.29 nm

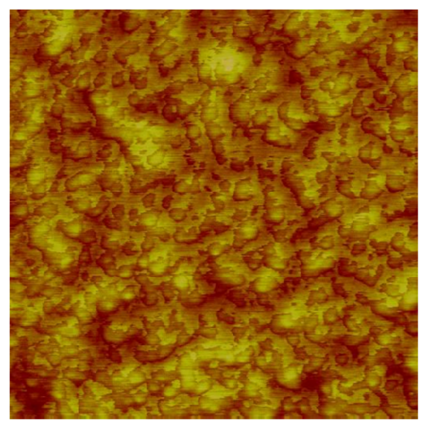
Not selected recipes



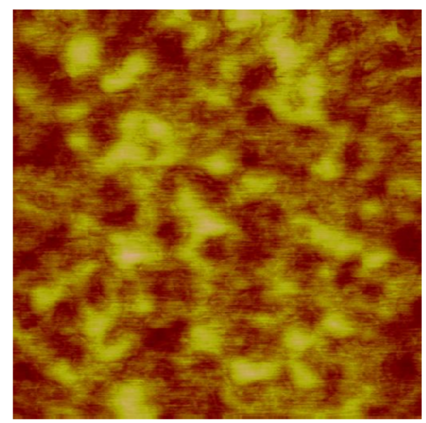
High bias
RMS: 0.59 nm



High pressure
RMS: 0.53 nm



Cl_2:N_2=1:1
RMS: 0.42 nm

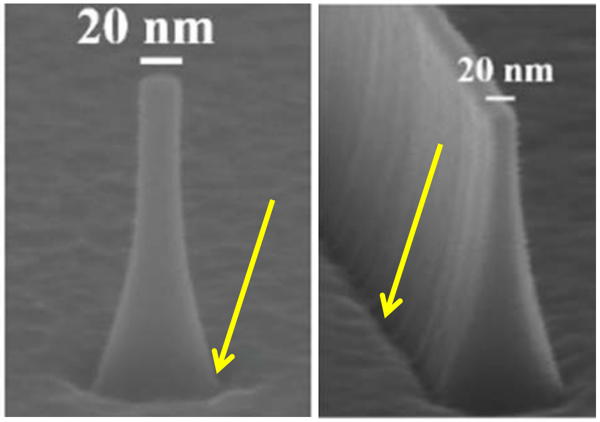


BCl_3-based chemistry
RMS: 0.56 nm

[Zhao EDL 2014]

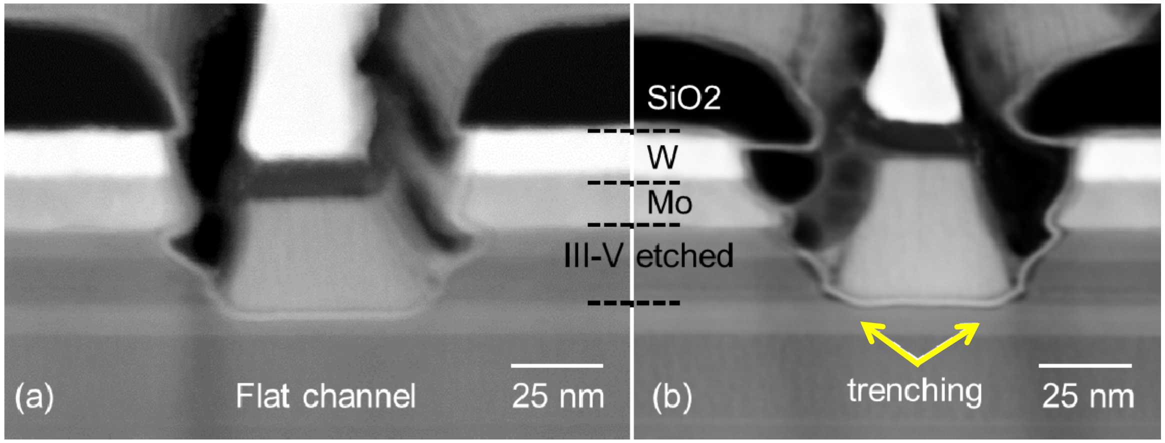
III-V dry etch: trenching

BCl_3-chemistry



[Zhao IEDM 2014]

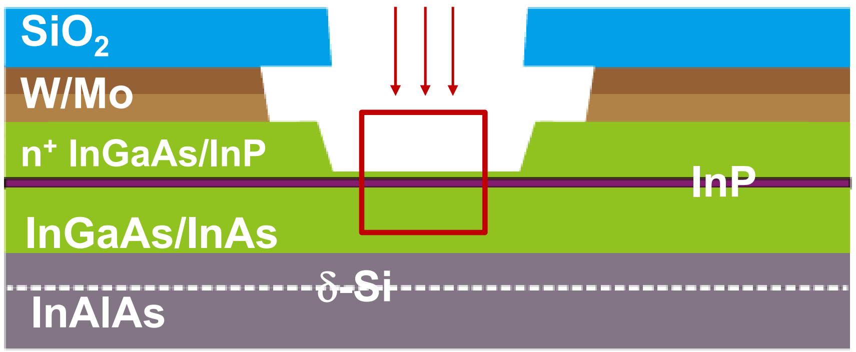
Cl_2:N_2-chemistry



Low bias High bias

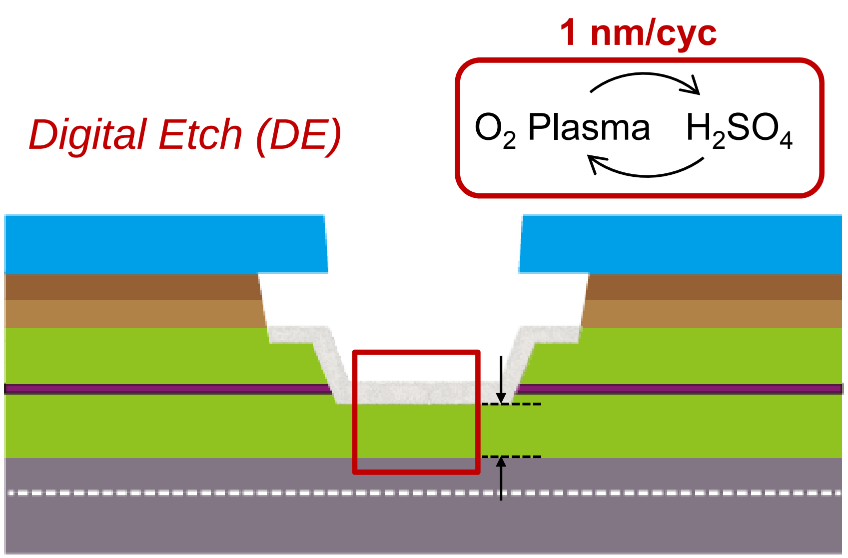
New III-V recess technology: Precise channel thickness (t_c) control

Cl_2 anisotropic RIE



- Anisotropic
- Accurate depth control

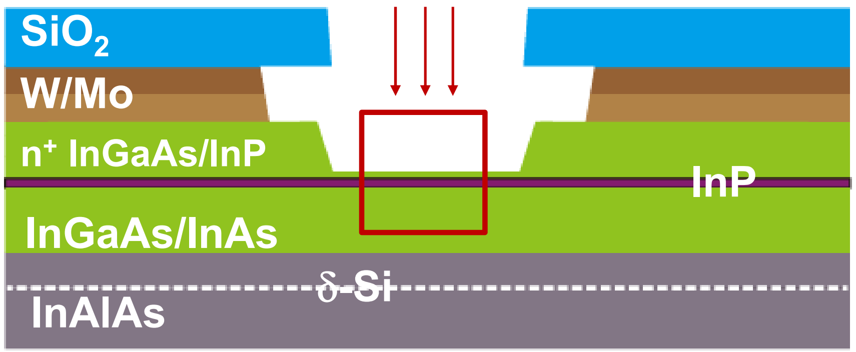
Digital Etch (DE)



[Lin, EDL 2014]

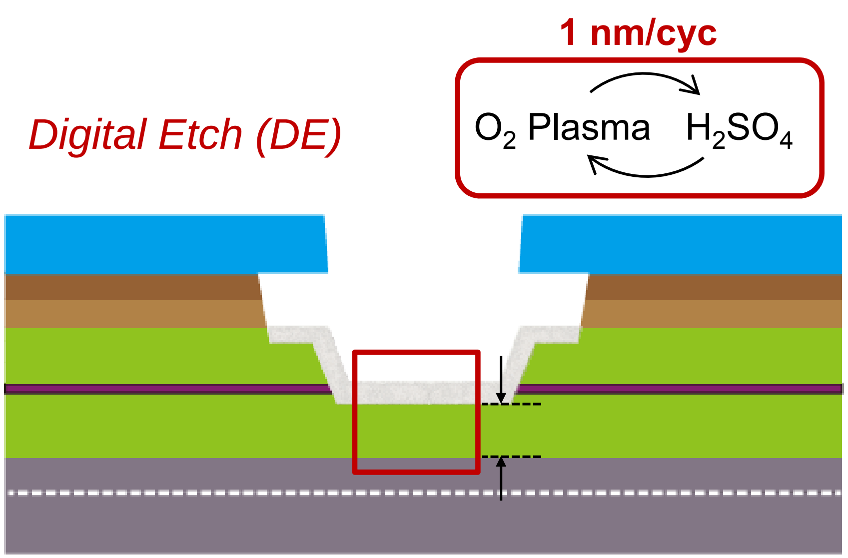
New III-V recess technology: Precise channel thickness (t_c) control

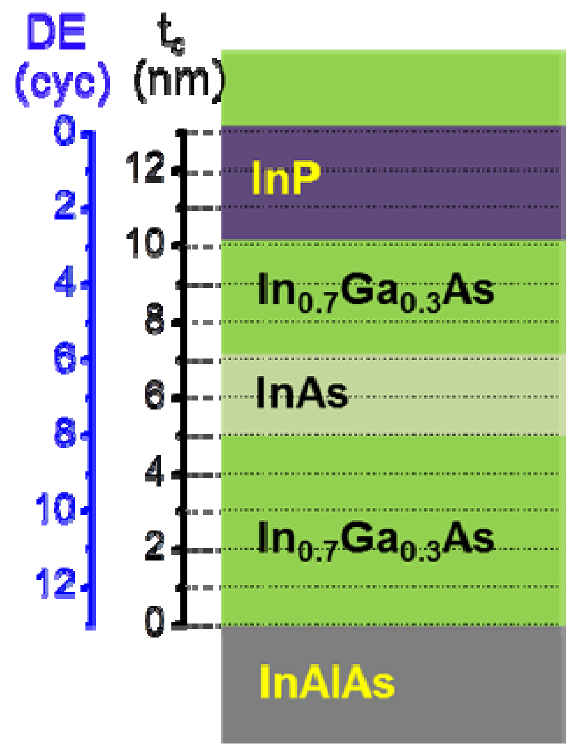
Cl_2 anisotropic RIE



- Anisotropic
- Accurate depth control
- Accurate and fast calibration

Digital Etch (DE)

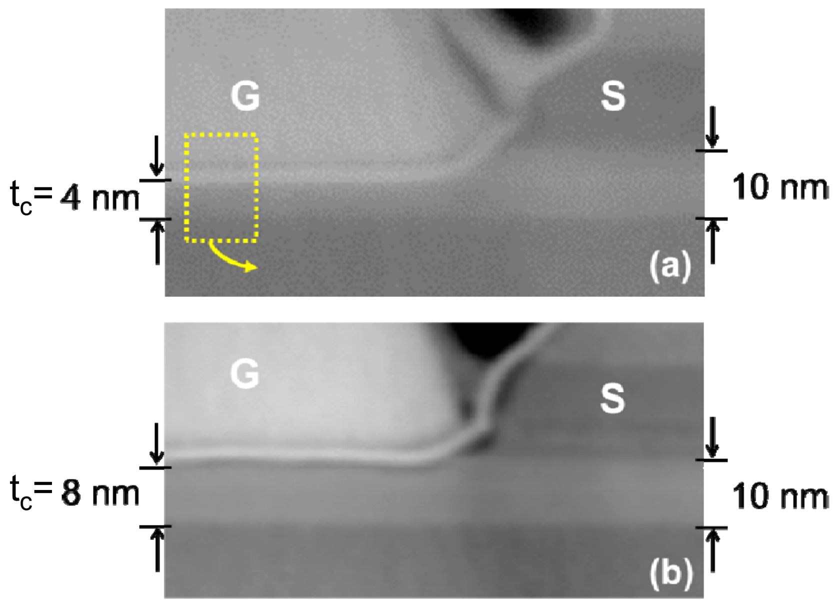


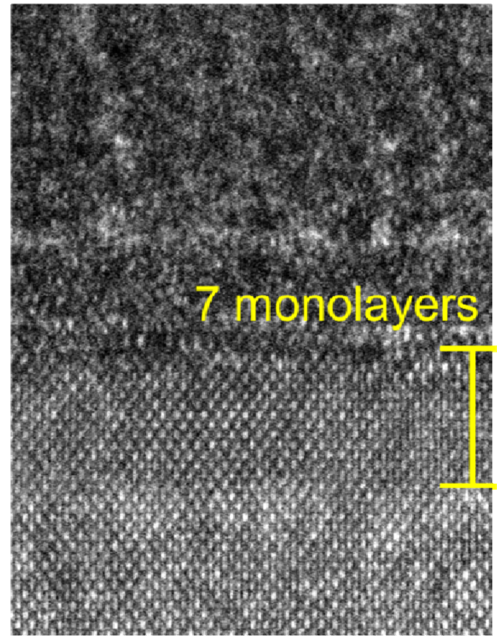


[Lin, EDL 2014]

Precise channel thickness (t_c) control

1 nm depth control

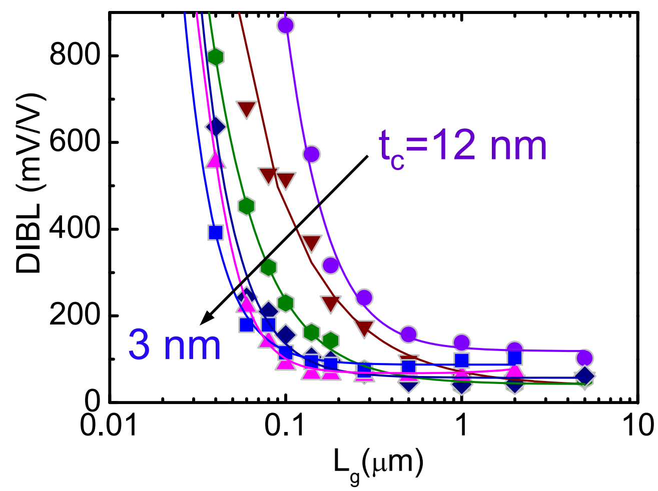




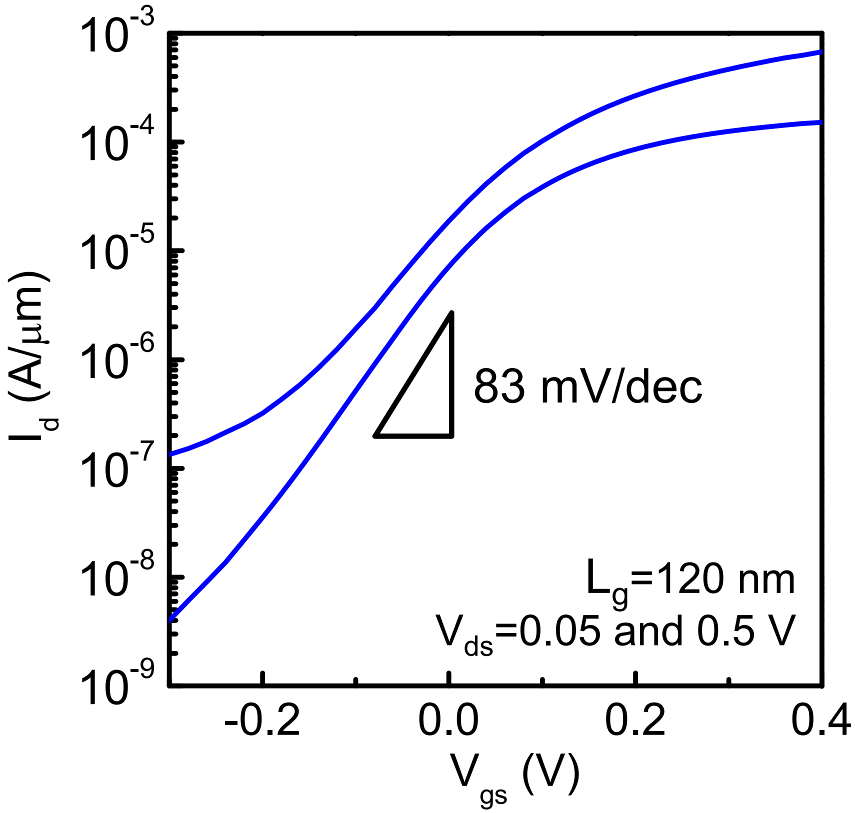
Device scaling study

- ON-state: I_{ON}, g_m, R_{SD}
- OFF-state: S, DIBL, V_t roll-off

[Lin, TED submitted]



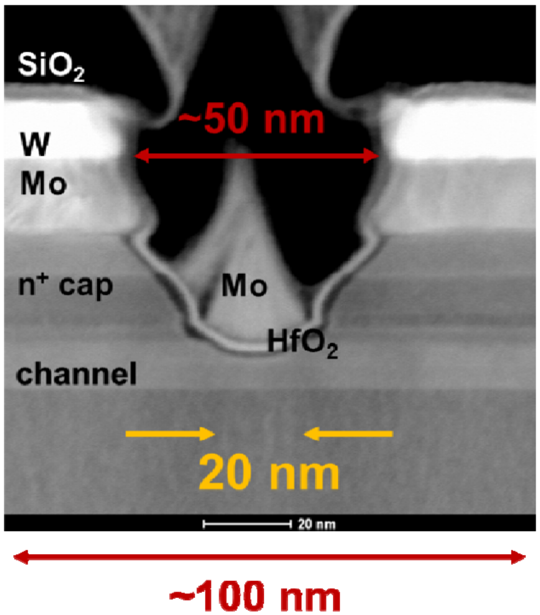
Typical long-channel characteristics

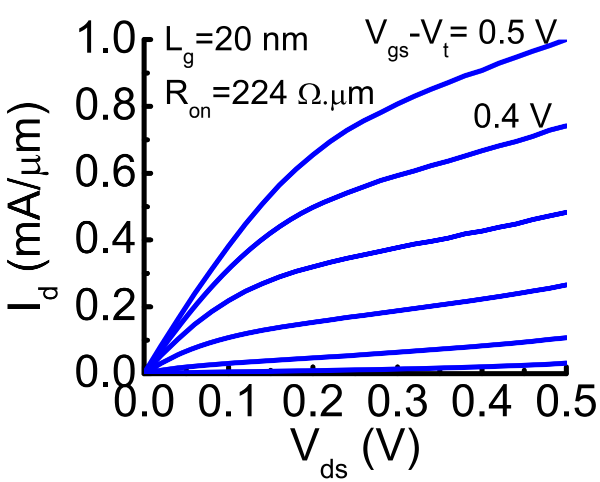


- Steep S at low V_{ds} → Low D_{it}
- $J_g < 10^{-2}$ A/cm^2 at EOT~0.5 nm → gate leakage suppression (typical HEMT: J_g>100 A/cm^2)

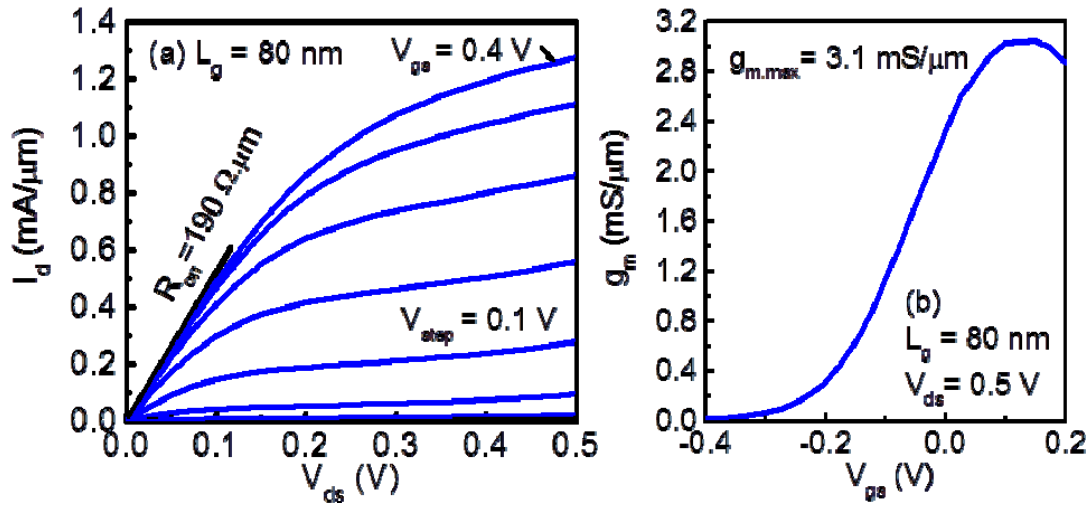
Scalability and performance

Scalability

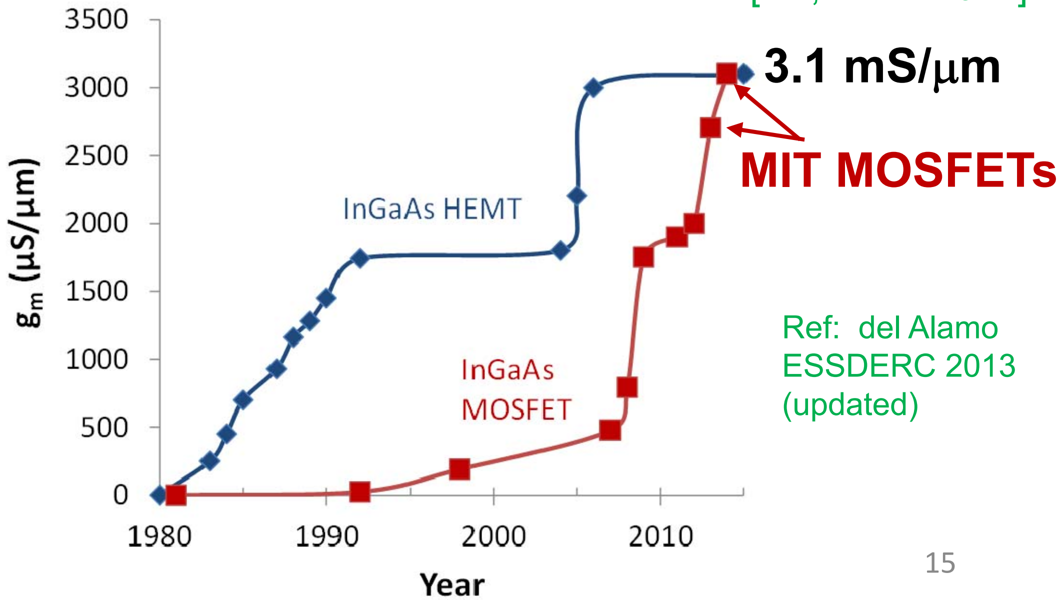




Performance



[Lin, IEDM 2014]



Ref: del Alamo
ESSDERC 2013
(updated)

Conclusions

- Scalable self-aligned InGaAs MOSFETs
  - CMOS manufacturability, performance, scalability
- Bilayer ohmic contact for footprint scaling
- III-V recess
  - III-V dry etch: smooth surface and no trenching
  - Digital etch: accurate depth control
- InGaAs MOSFET performance analysis
  - Steep subthreshold swing: low D_{it}
  - Gate leakage suppression
  - Record transconductance achieved
  - Working L_g=20 nm InGaAs MOSFETs